

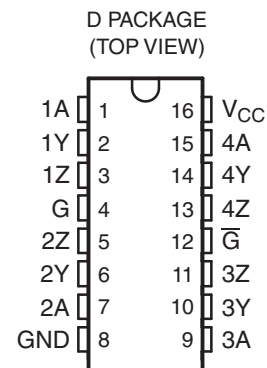
## LOW-VOLTAGE HIGH-SPEED QUADRUPLE DIFFERENTIAL LINE DRIVER WITH $\pm 15$ -kV IEC ESD PROTECTION

### FEATURES

- Meets or Exceeds Standards TIA/EIA-422-B and ITU Recommendation V.11
- Operates From a Single 3.3-V Power Supply
- ESD Protection for RS422 Bus Pins
  - $\pm 15$ -kV Human-Body Model (HBM)
  - $\pm 8$ -kV IEC61000-4-2, Contact Discharge
  - $\pm 15$ -kV IEC61000-4-2, Air-Gap Discharge
- Switching Rates up to 32 MHz
- Propagation Delay Time . . . 8 ns Typ
- Pulse Skew Time . . . 500 ps Typ
- High Output-Drive Current . . .  $\pm 30$  mA
- Controlled Rise and Fall Times . . . 5 ns Typ
- Differential Output Voltage With 100- $\Omega$  Load . . . 2.6 V Typ
- Accepts 5-V Logic Inputs With 3.3-V Supply
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Driver Output Short-Protection Circuit
- Glitch-Free Power-Up/Power-Down Protection

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Extended ( $-55^{\circ}\text{C}/105^{\circ}\text{C}$ ) Temperature Range<sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



(1) Additional temperature ranges are available – contact factory

### DESCRIPTION/ORDERING INFORMATION

The AM26LV31E is a quadruple differential line driver with 3-state outputs. This driver has  $\pm 15$ -kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and  $\pm 8$ -kV ESD (IEC61000-4-2, Contact Discharge) protection. This device is designed to meet TIA/EIA-422-B and ITU Recommendation V.11 drivers with reduced supply voltage.

The device is optimized for balanced-bus transmission at switching rates up to 32 MHz. The outputs have high current capability for driving balanced lines, such as twisted-pair transmission lines, and provide a high impedance in the power-off condition.

The AM26LV31ES is characterized for operation from  $-55^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ .

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^{\circ}\text{C}$ to $105^{\circ}\text{C}$	SOIC – D	Tape and reel	AM26LV31ESDREP	A26LV31ESP

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



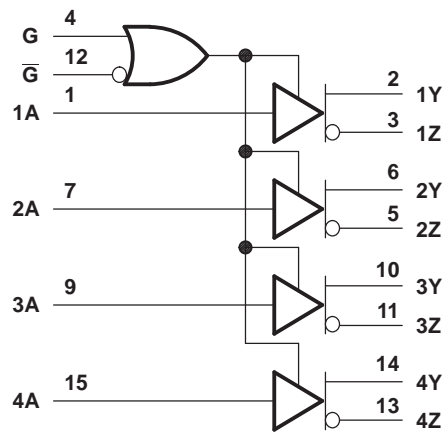
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE<sup>(1)</sup>

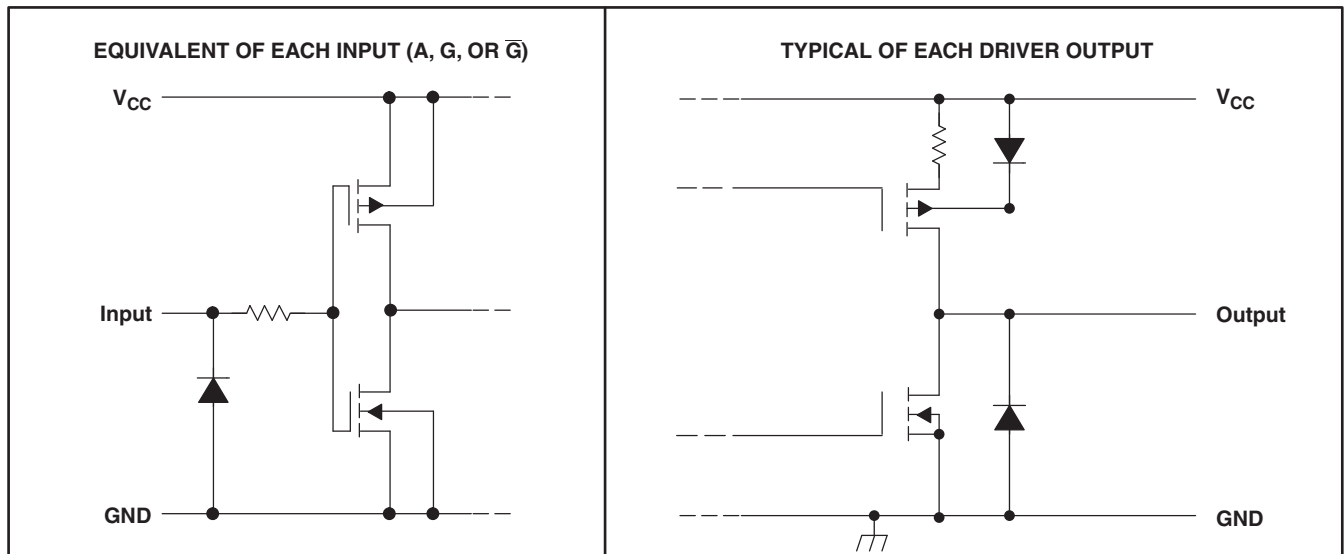
INPUT A	ENABLES		OUTPUTS	
	G	$\bar{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

LOGIC DIAGRAM



SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
$V_{CC}$	Supply voltage range <sup>(2)</sup>	-0.5	6	V
$V_I$	Input voltage range	-0.5	6	V
$V_O$	Output voltage range	-0.5	6	V
$I_{IK}$	Input clamp current	$V_I < 0$		-20 mA
$I_{OK}$	Output clamp current	$V_O < 0$		-20 mA
$I_O$	Continuous output current		±150	mA
	Continuous current through $V_{CC}$ or GND		±200	mA
$T_J$	Operating virtual junction temperature		150	°C
$\theta_{JA}$	Package thermal impedance <sup>(3)(4)</sup>		73	°C/W
$T_A$	Operating free-air temperature range	-55	105	°C
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential input voltage are with respect to the network GND.
- (3) Maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(max)} - T_A)/\theta_{JA}$ . Selecting the maximum of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	3	3.3	3.6	V
$V_I$	Input voltage	0		5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			-30	mA
$I_{OL}$	Low-level output current			30	mA
$T_A$	Operating free-air temperature	-55		105	°C

## ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	$V_{IH} = 2\text{ V}, V_{IL} = 0.8\text{ V}, I_{OH} = -20\text{ mA}$			V
$V_{OL}$	Low-level output voltage	$V_{IH} = 2\text{ V}, V_{IL} = 0.8\text{ V}, I_{OL} = 20\text{ mA}$			V
$ V_{OD1} $	Differential output voltage	$I_O = 0\text{ mA}$			V
$ V_{OD2} $	Differential output voltage	$R_L = 100\ \Omega$ (see Figure 1) <sup>(2)</sup>			V
$\Delta V_{OD} $	Change in magnitude of differential output voltage	$R_L = 100\ \Omega$ (see Figure 1) <sup>(2)</sup>			V
$V_{OC}$	Common-mode output voltage	$R_L = 100\ \Omega$ (see Figure 1) <sup>(2)</sup>			V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage	$R_L = 100\ \Omega$ (see Figure 1) <sup>(2)</sup>			V
$I_{O(OFF)}$	Output current with power off	$V_{CC} = 0, V_O = -0.25\text{ V or } 5.5\text{ V}$			$\mu\text{A}$
$I_{OZ}$	High-impedance state output current	$V_O = -0.25\text{ V or } 5.5\text{ V}, G = 0.8\text{ V or } \overline{G} = 2\text{ V}$			$\mu\text{A}$
$I_I$	Input current	$V_{CC} = 0\text{ or } 3.6\text{ V}, V_I = 0\text{ or } 5.5\text{ V}$			$\mu\text{A}$
$I_{OS}$	Short-circuit output current	$V_O = V_{CC}\text{ or GND}$ <sup>(3)</sup>			mA
$I_{CC}$	Supply current (total package)	$V_I = V_{CC}\text{ or GND}, \text{ No load, enable}$			$\mu\text{A}$
$C_{pd}$	Power dissipation capacitance	No load <sup>(4)</sup>			pF

(1) All typical values are at  $V_{CC} = 3.3\text{ V}, T_A = 25^\circ\text{C}$ .

(2) Refer to TIA-EIA-422-B for exact conditions.

(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

(4)  $C_{pd}$  determines the no-load dynamic current consumption:  $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

## SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PHL}$	Propagation delay time, high- to low-level output	See <a href="#">Figure 2</a>	4	8	12	ns
$t_{PLH}$	Propagation delay time, low- to high-level output		3.5	8	12	ns
$t_t$	Transition time ( $t_r$ or $t_f$ )	See <a href="#">Figure 2</a>		5	10	ns
$t_{PZH}$	Output-enable time to high level	See <a href="#">Figure 3</a>		10	20	ns
$t_{PZL}$	Output-enable time to low level	See <a href="#">Figure 4</a>		10	20	ns
$t_{PHZ}$	Output-disable time from high level	See <a href="#">Figure 3</a>		10	20	ns
$t_{PLZ}$	Output-disable time from low level	See <a href="#">Figure 4</a>		10	20	ns
$t_{sk(p)}$	Pulse skew	See <a href="#">Figure 2</a> <sup>(2)(3)</sup>		0.5	3	ns
$t_{sk(o)}$	Skew limit (pin to pin)				1.5	ns
$t_{sk(lim)}$	Skew limit (device to device)				3	ns
$f_{(max)}$	Maximum operating frequency	See <a href="#">Figure 2</a>		32		MHz

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

(3) Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

## ESD PROTECTION

PARAMETER	TEST CONDITIONS	TYP	UNIT
Driver output	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

PARAMETER MEASUREMENT INFORMATION

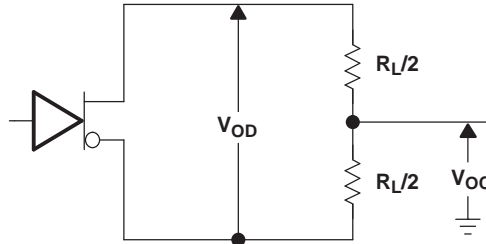
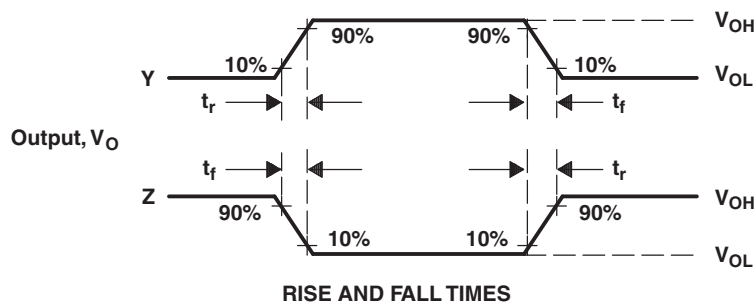
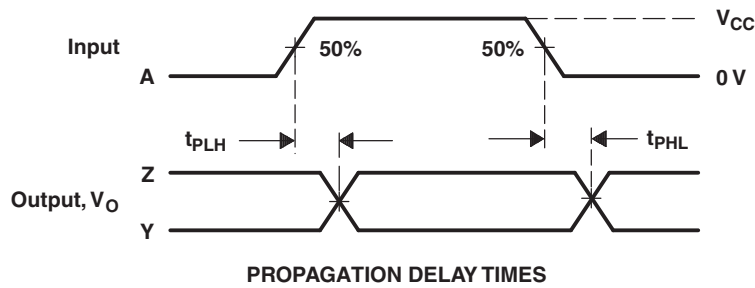
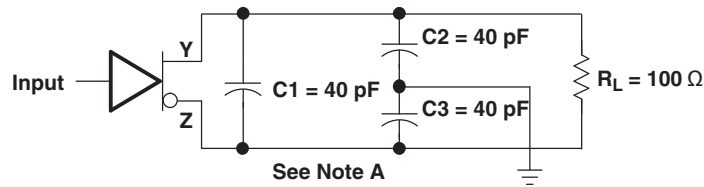


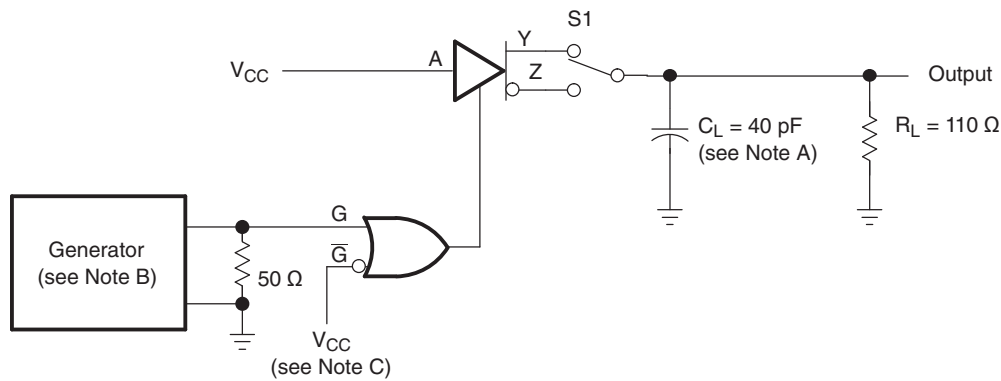
Figure 1. Test Circuit,  $V_{OD}$  and  $V_{OC}$



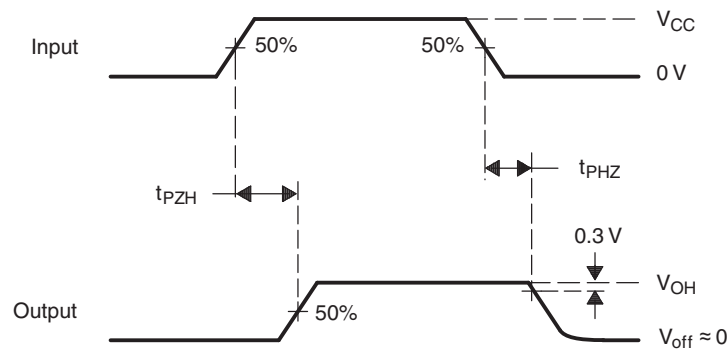
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics: PRR = 32 MHz, 50% duty cycle,  $t_r$  and  $t_f \leq 2$  ns.

Figure 2. Test Circuit and Voltage Waveforms,  $t_{PHL}$  and  $t_{PLH}$

PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT

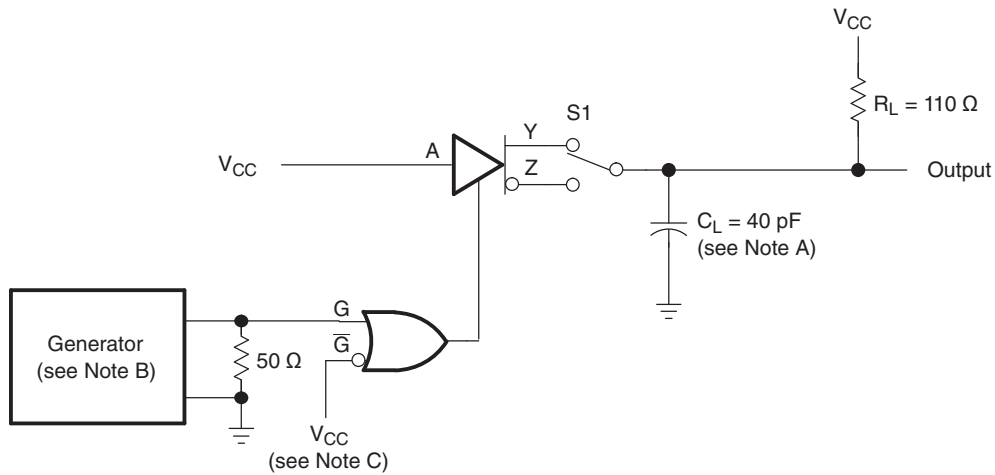


VOLTAGE WAVEFORMS

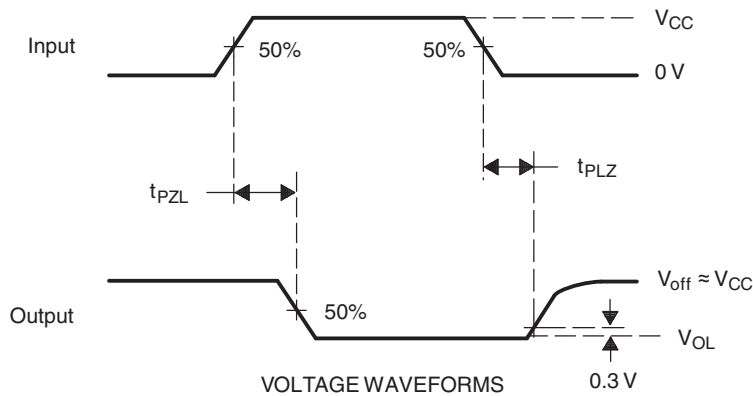
- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%,  $t_r = t_f \leq 2\text{ns}$ .
- C. To test the active-low enable  $\bar{G}$ , ground G and apply an inverted waveform  $\bar{G}$ .

Figure 3. Test Circuit and Voltage Waveforms,  $t_{PZH}$  and  $t_{PHZ}$

PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%,  $t_r = t_f \leq 2\text{ns}$ .
- C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform  $\overline{G}$ .

Figure 4. Test Circuit and Voltage Waveforms,  $t_{PZL}$  and  $t_{PLZ}$



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
AM26LV31ESDREP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/09603-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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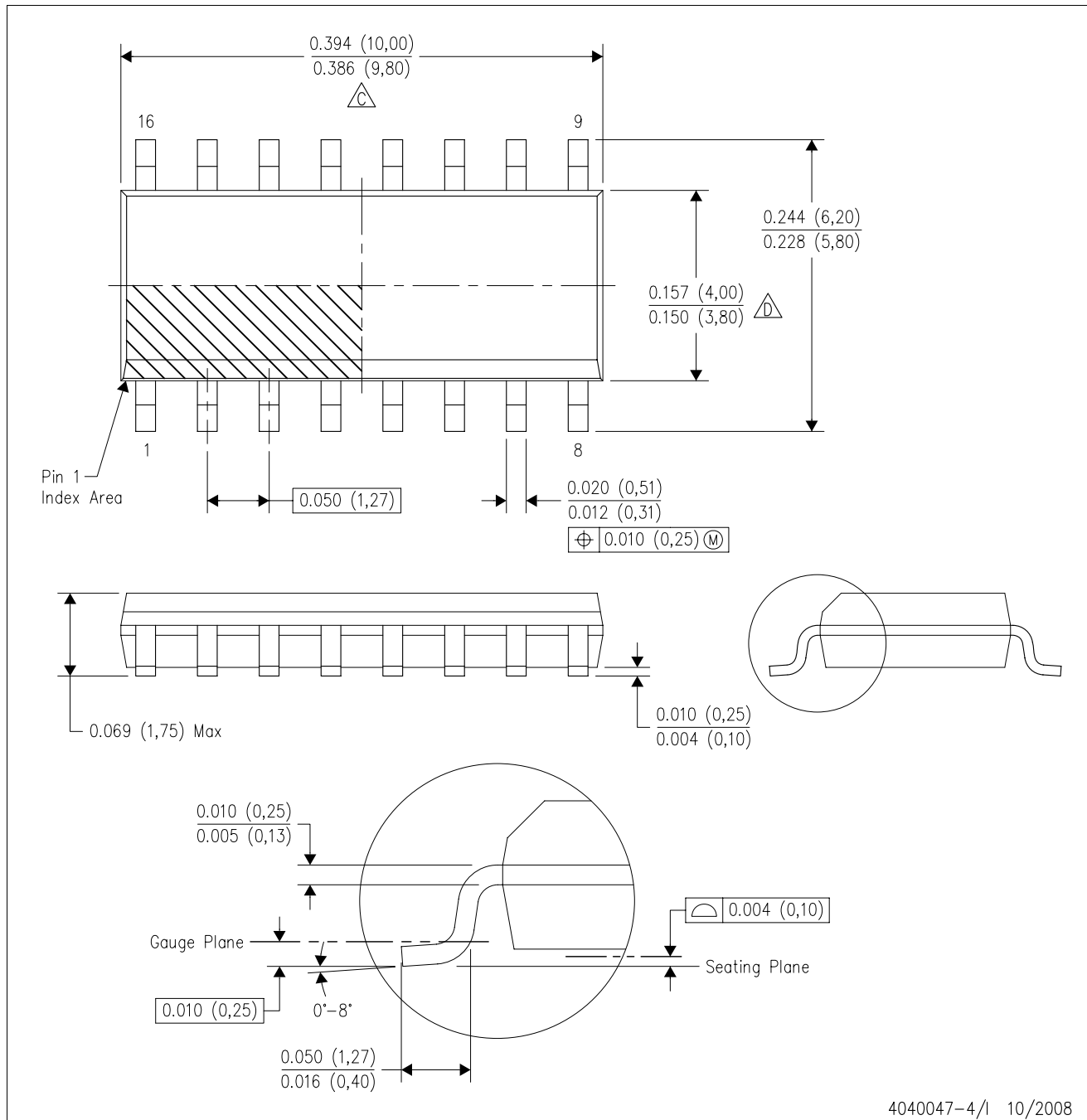
- Catalog: [AM26LV31E](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

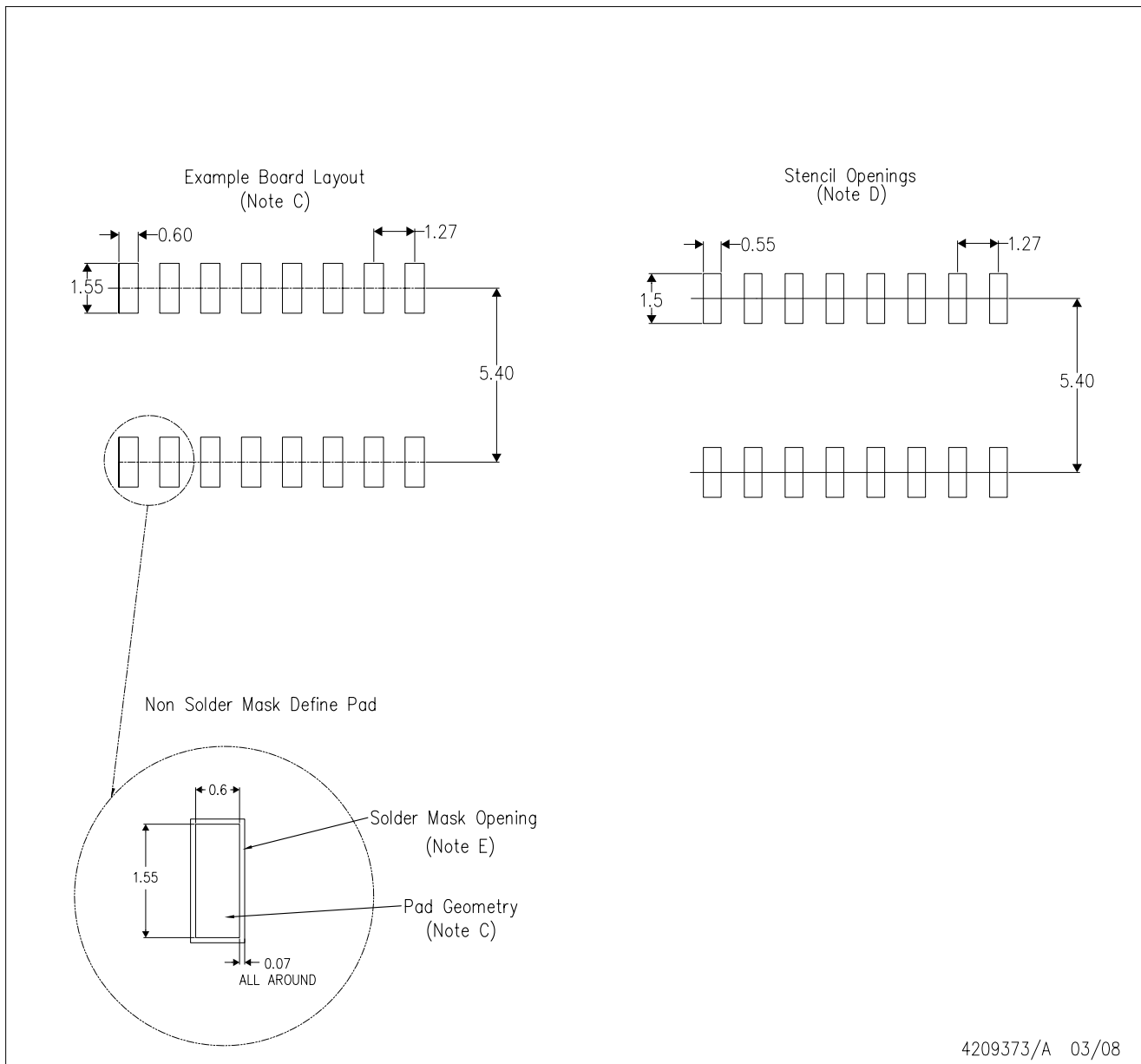
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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